1553 RT STATUS WORD

cPCI – PCI – PC104-SBC

The internal CRAM Status Word is divided in two segments:

1- Bits 0 to 5 define response time – Class A or B, Transmit Shutdown (A or B) from 1553 MODE commands and transmits error injection.
2- Bits 6-15 are directly inserted into 1553 CRAM-RT status word bus answer.

The CRAM reads from RT block the “current_status” register and refreshed the internal register after every BC enquire.

Default: 0 – disable 1- enable

Bit 0 – CLASS A – '1' CLASS B –'0' – Default – Internal

Bit 1 – Shut down channel A – Internal

Bit 2 – Shut down channel B – Internal

Bit 3 – reserved

Bit 4 – Parity error Injection (ODD Parity)

Bit 5 – Sync Manchester Error Injection

Bit 6 – Instrumentation – Status Word

Bit 7 – Service Request – Status Word

Bit 8 – Reserved – Status Word

Bit 9 – Reserved – Status Word

Bit 10 – Reserved – Status Word

Bit 11 – Reserved – Status Word

Bit 12- Busy – Status Word

Bit 13 – S_Flag – Status Word

Bit 14 – Din – Status Word

Bit 15 – T_Flag – Status Word

INTERNAL RECEIVE STATUS REGISTER

This register analyzes bus errors. It is refreshed every frame and is stored according to the mode to the following registers:

1- RT MODE - “Status_Bit” from RT block,

2- BC MODE – “error_detect” from BC block

3- BM or BCBM or RTBM MODES at the end of receive data structure.

4-

Default: 0 – disable 1- enable

Bit 0 – Parity Command Error

Bit 1 – Parity Data Error

Bit 2 – Sub-address Error

Bit 3 – Frame with more than two words and two command syncs

Bit 4 – Mode Command Sub-Address 0 or 31

Bit 5 – Mode Code Error

Bit 6 – Mode Code Error

Bit 7 – Manchester Code

Bit 8 – Number Data Error – last 5 bits in the BC-RT Command

Bit 9 – Sync Error – Command or Data

Bit 10 – RT_RT Selected – two words with two sync command

Bit 11 – Com_OV_Error – too many sync commands

Bit 12- Data_OV_error – too many command sync

Bit 13 – T/R bit broadcast error – incorrect bit inside BROADCAST command

Bit 14 – T/R bit error – incorrect bit inside BC-RT command

Bit 15 – Sync First Sample – 0- Command 1-Data

Error Mask Register

The register set which errors the CRAM will set Status error Bit or Mask Status Transmission.

// ERROR REGISTER LIST
1- enable 0 – disable Default:

Bit 0 – Manchester Signal Error (Sync or Error)

Bit 1 –Incorrect T/R Broadcast Bit Error

Bit 2 – Incorrect T/R Data transmission error (BC-RT command)

Bit 3 – Mode Code Error *

Bit 4 – Incorrect Number of data transmitted

Bit 5 – Long Loop Test Error **

Bit 6 – Too many Command syncs error

Bit 7 – More than 32 data words

Bit 8 – Command Sync Error

Bit 9 – Parity Data error

Bit 10 – Parity Command Err

Bit 11 – NOT selected RT Sub address Error

Bit 12

Bit 13

Bit 14- Enable Error Status Bit if occurred any of the above errors

Bit 15 – Fatal Status RT mask – IF set mask RT Status transmission if occurred any of the above errors.

*** RT mode control is defined when sub address is 0 or 31. Technically can be up to 32 combinations for transmit or receive (T/R bit) however the standard defines that the first 16 combinations are transmission commands from 16 to 20 has a single T/R bit option as defined on table XXXXXXXX. . If the unit receive any of the above error conditions and the bit is set.**

**** Many systems use the long loop test (LLT) procedure to test RTs. It use sub address 30 to transmit or receive 32 predefined words. If the BC transmit less than 32 words this bit is set.**

RT -SELECT SUBADDRESS REGISTERS

Sub-address 0-15 and 16-31

These registers can be used in the RT mode to indicate frame message for unused RT subsystems. The error register can enable or disable to set the RT Status Error Bit when the error frame is received by the RT. Registers “sa_mask[2]” in the RT block is load into the internal register during RT initialization, when the host send a new command or change the RT address in the RT control block.

RT -SELECT REGISTERS

RTs 0-15 and 16-31

These registers select which RTs frames should be stored in the memory in the Bus Monitor mode.. Registers “mrt_ena_dis [2]” in the BMRT block is load into the internal register during bus monitor mode initialization..