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Rev. 3.5 May 01, 2008

INTRODUCTION TO THE UADI SYSTEM

DESCRIPTION

The UADI-ARTIC-RS-1553 is a compact, MIL-STD-1553 compliant, transmit/receive interface board for use as a single board computer. BMC supplies programs with source code in C and the user implement his application.

FEATURES

The UADI-ARTIC-RS--1553 board offers the following features:

- **Works as a Bus Controller, Remote Terminal and Bus Monitor**
- **Powerful 16 bit microcontroller for intelligent Real-Time operation**
- **1553 BC-RT-BM Operating Modes**
- **Fully software programmable MIL-STD-1553 parameters**
- **Receive and transmit counters**
- **ARINC programmable parameters: Parity, baud rate,etc**
- **Independently programmable Transmit and Receive Buffer sizes**
- **RS232 programmable parameters: Parity, baud rate, etc**
- **8 General 3.3V I/O**

SPECIFICATIONS

Dimensions:

3.8" X 3.6"

Power Requirements:

+5 Volts @ 350 mA max. (1553- 50% DUTY CYCLE per channel)
Standby Operation +5 Volts @ 50 mA

Data Transfer Rate:

MIL-STD-1553 1 MBYTES P/SECOND
ARINC UP TO 1 MBYTES P/SECOND
RS232 UP TO 250 KHZ

SOFTWARE

An Application Program Interface (API) is included. This interface consists of a library of high-level language functions that allow the user to write custom applications programs without having to understand the "nuts and bolts" of the UADI-ARTIC-RS-1553 system. When using the API, a user need not concern himself with the settings of the individual bits of the MIL-STD-1553 words, nor with the word ordering and timing prescribed by the standard; these tasks are handled automatically by the system software.

APPLICATIONS

The UADI-ARTIC-RS-1553 may be used for many types of testing and simulation operations. The system may be configured as a Bus Controller, Remote Terminal, or Bus Monitor. Within each of these categories, flexibility is given to the user to custom tailor the most suitable test program for his needs

UADI-ARTIC-RS-1553 OPERATION.

The UADI-1553 has an internal memory of 1kx16. This memory is used for data transmission.
BC mode requires the user store data to be transmitted at any location in segments of 64 words. The user loads the size with the memory location in a internal register and immediately the BC start to transmit.
RT mode used the memory as data response for a BC command. Each sub address has 32 words. A total of 1024 words; 32 sub addresses each with 32 words.

Example for RT sub address data stored:

```
for (i=0 ; i<range; i++)
{
      Address = sub_address * 32 + i ;
   WriteDPM ( Address, (char *)&data to be stored, 1) ;
}
```

UADI-1553 CONTROL WORD

The internal UADI-1553- Control register defined UADI operational mode

Default: 0 – disable 1- enable
Bit 0 –Internal Master Reset
Bit 1 –Reserved – keep value high
Bit 2 – Parity Error Injection
Bit 3 – External LED on board
Bit 4 – BM operational Mode
Bit 5 – RT operational mode
Bit 6 – Service Request – RT Status Word bit
Bit 7 – BC mode*
Bit 8 – RT ADDRESS 0
Bit 9 – RT ADDRESS 1
Bit 10 – RT ADDRESS 2
Bit 11 – RT ADDRESS 3
Bit 12 - RT ADDRESS 4
Bit 13 – Select transmit channel: A – "0" B- "1"
Bit 14 – Shut down transmit channel A
Bit 15 – Shut down transmit channel B

* Not available in all units

INTERNAL 1553- RECEIVE STATUS REGISTER

This register analyzes bus errors. It is refreshed every frame and is stored according to the mode to the following registers:

Bit 0 – Parity Command Error
Bit 1 – Parity Data Error
Bit 2 – Reserved
Bit 3 – Broadcast
Bit 4 – Mode Command Sub-Address 0 or 31
Bit 5 – Data Receive channel -0 : A 1:B
Bit 6 – RT-RT receive command
Bit 7 – Manchester Code Error
Bit 8 – Number Data Error – last 5 bits in the BC-RT Command
Bit 9 – Fatal Error– Command error
Bit 10 – Error flag – RT mode Error bit is set
Bit 11 – Com_OV_Error – too many sync commands
Bit 12- Data_OV_error – receive more than 32 data words
Bit 13 – Manchester Data Error
Bit 14 – Mode Command legal error
Bit 15 – Sync First Sample – 0- Command 1-Data

RS232 CHANNELS

The SBC UADI board has two RS232 channels. The channels are embedded in the microcontroller MSP430F149/169 from TI. A detail explanation about the UART operation is available in the TI microcontroller data book.

INPUT/OUTPUT

The SBC UADI board has eight general I/O ports. The I/O ports are embedded in the microcontroller MSP430F149/169 defined as PORT 6. A detail explanation about the UART operation is available in the TI microcontroller data book.
Please note the maximum input signal should be 3.4 Volt.

Internal Jumpers

The FPGA can be programmed by the CPU (parallel) or by he PROM (serial) on board. Header JP7 specify if Data in comes from CPU or PROM. If the CPU is selected JP3 must be open.
Jumper J1 enable to program the CPU using the RS232 serial port.

UADI CONNECTORS

J2 - POWER CONNECTOR 4 PIN HEADER

PIN	1	+12V (NEED ONLY FOR ARINC DRIVERS)
PIN	2	-12 V (NEED ONLY FOR ARINC DRIVERS)
PIN	3	+5 VOLT
PIN	4	GND

H1 – RS232- 10 PIN HEADER(5X2) (SOLDER SIDE)

PIN	1	RT-ADD0
PIN	2	RxD (RS232 – RECEIVER SIDE)
PIN	3	TxD(RS232 – RECEIVER SIDE)/ RT-PARITY
PIN	4	DTR (RS232)
PIN	5	GND
PIN	6	RT-ADD4
PIN	7	RT-ADD3
PIN	8	RTS (RS232)/ RT-ADD2
PIN	9	RT-ADD1
PIN	10	NC

P2 – RS232- 3 PIN HEADER

PIN	1	GND (LEFT PIN)
PIN	2	RxD (RS232 – RECEIVER SIDE)
PIN	3	TxD(RS232 – RECEIVER SIDE)

P7 – 4 pin header – FIRST ARINC CHANNEL

PIN	1	ARINC 429 – TRANSMIT +
PIN	2	ARINC 429 – TRANSMIT -
PIN	3	ARINC 429 – RECEIVE +
PIN	4	ARINC 429 – RECEIVE -

P6 – 4 pin header –SECOND ARINC CHANNEL

PIN	1	ARINC 429 – TRANSMIT +
PIN	2	ARINC 429 – TRANSMIT -
PIN	3	ARINC 429 – RECEIVE +
PIN	4	ARINC 429 – RECEIVE -

P3 — 1553 CHANNEL A

PIN	1	1553 – CHANNEL A + (LEFT PIN – COMP. SIDE)
PIN	2	1553 – CHANNEL A -

P4 — 1553 CHANNEL B

PIN	1	1553 – CHANNEL B + (LEFT PIN – COMP. SIDE)
PIN	2	1553 – CHANNEL B -

1553 Jumpers J3 & J4 – (SOLDER SIDE)

JUMPER	1-2	7-8	(External jumpers)	-DIRECT COUPLING
JUMPER	3-4	5-6	(Internal jumpers)	- TRANSFORMER COUPLING

4 PIN HEADER(2X2) (CLOSE TO U4)

PIN	1-2	SHORT REQUIRED FOR RS-232 SOFTWARE DOWNLOAD
PIN	3-4	SHORT REQUIRED FOR RS-232 SOFTWARE DOWNLOAD

H5 – 16 PIN HEADER(2X8) –SOLDER SIDE
Two columns – odd- signals even-ground

The signals of H5 are connected directly to port 6 CPU I/O. These signals can be defined as Analog Inputs or regular I/O according to user definitions. The signals are located in the internal connector pins

PIN 1- connected to Port 6.0

PIN 3 (second pin in the column) – connected to Port 6.1

……

Pin 15 (eight pin in the column) – connected to Port 6.7